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MULTI-LAYER CAPACITOR AND METHOD FOR MANUFACTURING THE SAME

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FIELD OF THE INVENTION

The present invention relates to a multi-layer capacitor formed of a dielectric layer and a metal thin film layer, and a method for manufacturing the capacitor.

BACKGROUND OF THE INVENTION

Recently, all electronic components including a capacitor have been urgently required to be downsized and increased in performance. Capacity of the capacitor is proportional to an area of an electrode plate and is inversely proportional to a distance between electrodes. At this time, the thickness of a dielectric equals to the distance between the electrodes. When dielectrics have the same dielectric constant, for increasing the capacity of the capacitor, the area of the electrode plate needs to be increased or the dielectric layer needs to be thinned. In other words, for downsizing the capacitor and simultaneously keeping or increasing the capacity thereof, it is effective to thin the dielectric layer and increase an effective area of the electrode plate. As a laminated body that is formed of the dielectric layer and the metal thin film layer and is used in the capacitor or the like, a film capacitor is known. The structure of the film capacitor is described below. A metal thin film made of aluminum or the like is firstly formed on a resin film in a vacuum deposition method or a sputtering method. The resin film is made of polyester (for example, PEN or PET), polyolefin (for example, PP), or PPS. Metal thin films manufactured in such a method are laminated or wound, thereby forming the film capacitor. The resin film functions as a dielectric. In this case, constraint in

manufacturing the film limits thinning of the resin film. The minimum thickness of a film for a presently used film capacitor is about 1.2 μm. For further increasing the capacity of the capacitor, the effective area of the dielectric needs to be increased, namely the number of laminations and the number of turns need to be increased. However, simultaneous downsizing and capacity increase of the film capacitor reach the limit. While, U.S. Patent No. 5,125,138 discloses a multi-layer capacitor in which the laminated body is formed of a dielectric layer and a metal thin film layer and the thickness of the dielectric layer is about 1 μm. The dielectric layer is formed by polymerizing reactive monomer. Japanese Patent Unexamined Publication No. H11-147279 discloses a chip capacitor having a dielectric layer formed by polymerizing reactive monomer. Fig. 6 is a sectional view showing a structure of a conventional multi-layer chip capacitor.

In Fig. 6, internal electrodes 11 and dielectric layers 12 are sequentially laminated, and electric insulation part 13 exists in each internal electrode 11 every two layers. External electrodes 41 are finally formed to constitute the multi-layer chip capacitor as a product. Electric insulation parts 13 are provided for forming a capacitor. Electric insulation parts 13 function for preventing a short circuit and increasing the effective area of the dielectrics in a capacitor forming part.

Electric insulation parts 13 have no metal layer, so that uneven parts occur in the capacitor in response to the increase of the number of layers. This state is shown in the enlarged view of electric insulation parts 13 of Fig. 7. When the number of layers exceeds 1000, electric insulation parts 13 can be deeply recessed as shown in Fig. 8. In such a case, each internal electrode 11 is disconnected or internal electrodes 11 are short-circuited, thereby damaging the function as the capacitor. This problem can be further noticeable when the thickness of the dielectric layers is decreased to a thickness unachievable in the conventional film capacitor. The present invention aims to essentially address the problem occurring in achieving the downsizing or high capacity. The improvement of the productivity is also one of purposes of the present invention.

SUMMARY OF THE INVENTION

The present invention provides a multi-layer capacitor in which a plurality of dielectric layers and metal electrode layers are sequentially laminated. Metal electrode layers alternately have an electric insulation part. The dielectric layers cover and flatten recessed parts in the metal electrode layers produced by the electric insulation parts.

The present invention provides a method of manufacturing the multi-layer capacitor. The method comprises the following processes:

a monomer deposition process of forming a dielectric layer on a surface of a can roller rotating in a constant direction in the same vacuum chamber;

a patterning process of supplying patterning material to a part that corresponds to the electric insulation part and lies on the surface of the dielectric layer, and forming the electric insulation part;

a metal deposition process of forming a metal electrode layer on a surface of the dielectric layer except the electric insulation part; and

a flattening process of flattening a recessed part generated by the electric insulation part of a laminated body that is formed by repeating the processes discussed above.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a manufacturing apparatus of a multi-layer capacitor of the present invention.

Fig. 2A to Fig. 2C show a manufacturing process in accordance with exemplary embodiment 1 of the present invention.

Fig. 3A to Fig. 3C show a manufacturing process in accordance with exemplary embodiment 2 of the present invention.

Fig. 4A to Fig. 4C show a manufacturing process in accordance with exemplary embodiment 3 of the present invention.

Fig. 5 is a sectional view illustrating a form having different laminating positions of the present invention.

Fig. 6 is a sectional view illustrating a structure of a conventional multi-layer capacitor.

Fig. 7 is a sectional view illustrating an enlarged electric insulation part of the conventional multi-layer capacitor.

Fig. 8 is a perspective view illustrating the electric insulation part of the conventional multi-layer capacitor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Exemplary embodiments of the present invention will be hereinafter described with reference to the accompanying drawings. The accompanying drawings are pattern diagrams and do not show respective positions in accurate size.

Fig. 1 shows a manufacturing apparatus of a multi-layer capacitor of the present invention. Metal deposition source 4 is disposed under can roller 1 that rotates in the arrow direction in Fig. 1 at a constant angular velocity or a constant circular velocity. Metal electrode surface treating unit 7, monomer evaporation source 2, curing unit 8, resin surface treating unit 9, patterning material supplying unit 3 are disposed sequentially in the rotation direction of can roller 1 from the downside thereof. These units are engaged with vacuum chamber 5, and the inside of the chamber is held with vacuum by vacuum pump 6. The outer peripheral surface of can roller 1 is finished smoothly and specularly, and preferably cooled to -20 to 40 °C, especially preferably to -10 to 10 °C. The rotational speed can be set arbitrarily, but is preferably within a range of 15 to 70 rpm. Metal deposition source 4 has a shutter (not shown) facing to the surface of can roller 1 so as to control an interval of metal deposition. A metal electrode layer is thus formed on the surface of a dielectric layer. As the metal for the deposition, at least one selected from a group of Al, Cu, Zn, Sn, Au, Ag, and Pt, for example, is employed. The metal electrode may be formed in a sputtering method or the like instead of the vacuum deposition method. Metal electrode surface treating unit 7 performs an improving treatment of adhesiveness between a metal electrode surface and a

dielectric resin layer. For example, titanium atoms are deposited on the metal electrode surface in the sputtering method or the vacuum deposition method. Chemical bond of metal (electrode) · Ti · carbon (resin) is formed as a result.

The adhesiveness between resin and metal can be thus improved. A similar effect can be obtained also by a chemical vapor deposition (CVD) method using $TiCl_4$ or the like as raw material. When coupling material is added to the metal electrode, the coupling material segregates on an interface between the metal and the dielectric with heat treatment performed in a subsequent process of forming the laminated body. Chemical bond similar to that discussed above can be therefore obtained and adhesiveness can be improved. When light energy equivalent to polymerizing energy of reactive monomer is radiated, bonding of a polymerization starting part is broken and chemical bond of metal · carbon (resin component) is formed. An effect similar to that in the case where the coupling material is deposited on the metal surface can therefore be obtained. Monomer evaporation source 2 evaporates and vaporizes the reactive monomer toward the surface of can roller 1. A shutter (not shown) is disposed so as to control the deposition interval of the reactive monomer on can roller 1. The reactive monomer is deposited, and finally a dielectric layer is formed. The deposited reactive monomer is polymerized or cross-linked by curing unit 8 to form a resin thin film having a desired degree of cure. A polymerization initiator can be used additionally if necessary. As curing unit 8, for example, a radiating device of electron beams or ultraviolet rays is used. The resin thin film cured by curing unit 8 is surface-treated by resin surface treating unit 9. For example, oxygen plasma treatment or the like activates the resin surface. The adhesiveness to the metal thin film can be therefore improved. Patterning material supplying unit 3 deposits patterning material on the surface of the resin thin film in a band shape. No metal thin film is formed in a place having the deposited patterning material, and the place forms an electric insulation part in the laminated body. The laminating position of the electric insulation part is preferably displaced from a laminating position of an electric insulation part in the adjacent layer unit. As the patterning material, for example, oil or paraffin can

be employed. For supplying the patterning material, it is preferable to use a method of jetting the evaporated and vaporized patterning material from a nozzle and liquefying it on the surface of the resin thin film. A predetermined number of layer units including the resin layer and the metal layer are laminated on the outer peripheral surface of can roller 1, in the method discussed above. Here, the metal layer is laminated on the part other than a band-like electric insulation part. A cylindrical continuous body is thus formed. The continuous body is radially divided, for example, into eight parts every 45°, and removed from the can roller. Each divided body is then heated and pressed, thereby providing a flat parent element of the laminated body. The parent element is then cut to provide a laminated body in accordance with the manufacturing method of the present invention. According to the method discussed above, a laminated body can be manufactured efficiently and inexpensively by a simple method.

(Exemplary embodiment 1)

The manufacturing apparatus shown in Fig. 1 is used in exemplary embodiment 1. Fig. 2A to Fig. 2C show a manufacturing process of a multi-layer capacitor of the present invention. Degree of vacuum in vacuum chamber 5 is set at 2×10^{-2} Pa. The outer peripheral surface of can roller 1 is kept at 5°C. Dicyclopentadiene dimethanol diacrylate is used as the reactive monomer forming dielectric material. This is vaporized by monomer evaporation source 2 and deposited on the outer peripheral surface of can roller 1. As the reactive monomer, arbitrary material that is easily deposited and forms a good thin film after polymerization may be used. Polyfunctional acrylate, polyfunctional methacrylate, or polyfunctional vinyl ether is preferable.

Next, an electron-beam radiating device is used as curing unit 8, and cures the deposited dielectric material. At this time, the thickness of formed dielectric layer 12 is 0.1 μm. Resin surface treating unit 9 then applies the oxygen plasma treatment to the surface of dielectric layer 12. Patterning material supplying unit 3 supplies a patterning material to part corresponding to electric insulation parts

13. Fluorine-base oil is used as the patterning material. The patterning material is vaporized, jetted from a nozzle having a diameter of 50 μm, and adhered to the surface of dielectric layer 12 in a 150 μm-wide band shape. Metal deposition source 4 then deposits aluminum for forming internal electrode 11. Thickness of the deposited layer is 25 nm, and the surface resistance thereof is 6 Ω/square. Metal electrode surface treating unit 7 then deposits titanium by 0.1 nm in the sputtering method. The operations discussed above are repeated at 3000 times by rotating can roller 1. The process until now is called process A. Fig. 2A shows the state at the completion of process A. Next, a procedure of flattening electric insulation recessed part 14 is described. Electric insulation recessed part 14 is shown by a broken line. Since the recessed part is formed of dielectric material, the broken line is used for distinguishing between the dielectric materials. Metal deposition source 4 is firstly partitioned by a shutter, and monomer evaporation source 2 and curing unit 8 form resin layer 15 by repeating lamination and curing at about 500 to 1000 times. Monomer evaporation source 2 is then partitioned by a partition plate. Resin surface treating unit 9 etches resin layer 15 with oxygen plasma as shown in Fig. 2B. Electric insulation recessed part 14 is thus filled to flatten the surface of the laminated body as shown in Fig. 2C. Repeating the operations discussed above forms the laminated body having a thickness of about 1.6 mm. The obtained cylindrical laminated body is then radially divided into 20 and removed. A flat parent element of the laminated body is obtained by hot press. The element is cut, and then forms a chip capacitor as a product in a process similar to that for a conventional film capacitor. This process includes installation of an external electrode, for example. The obtained chip capacitor has 1.3 mm of thickness in the laminated direction, 1.6 mm of depth, and 3.2 mm of width (the direction between both external electrodes). The chip capacitor is small, but has 4.7 μF of capacity and 6.3 V of withstand voltage. The chip capacitor is mounted to a printed wiring board by solder. Any problem such as breakage of the laminated body or degradation of a capacitor characteristic does not occur.

(Exemplary embodiment 2)

A capacitor of exemplary embodiment 2 is manufactured using the apparatus shown in Fig. 1 in the same method as that of exemplary embodiment 1 until process A. Fig. 3A shows the state at the completion of process A. A procedure of flattening electric insulation recessed part 14 is described. Metal deposition source 4 is firstly partitioned by a shutter, and monomer evaporation source 2 and curing unit 8 form resin layer 21 by repeating the lamination and curing at about 500 to 1000 times. Monomer evaporation source 2 is then partitioned by a shutter, and resin surface treating unit 9 applies argon plasma to resin layer 21 as shown in Fig. 3B. At this time, a corner of the recessed part of resin layer 21 is firstly ground selectively, and finally resin layer 21 can fill the entire recessed part. The surface of the laminated body can be flattened as shown in Fig. 3C. Argon is used as inert gas in the present embodiment; however, the other inert gas such as xenon or neon may be used.

Repeating the operations discussed above forms the laminated body having a thickness of about 1.6 mm. A chip capacitor is obtained from the laminated body similarly to embodiment 1. This chip capacitor has a capacitor characteristic and solder heat resistance similar to those in embodiment 1.

(Exemplary embodiment 3)

A capacitor of exemplary embodiment 3 is manufactured using the apparatus shown in Fig. 1 in the same method as that of exemplary embodiment 1 until process A. Fig. 4A shows the state at the completion of process A. A procedure of flattening electric insulation recessed part 14 is described. Monomer evaporation source 2 is firstly partitioned by a shutter, and metal deposition source 4 is partitioned by shutter 31 having a pattern part. Metal layer 32 is passed through the pattern part and laminated at about 500 to 1000 times, as shown in Fig. 4B. Metal layer 32 fills the recessed part generated by the electric insulation part and flattens the surface of the laminated body, as shown in Fig. 4C. Repeating the operations discussed above forms the laminated body of about 1.6 mm. A chip

capacitor is obtained from the laminated body similarly to embodiment 1. This chip capacitor has a capacitor characteristic and solder heat resistance similar to those in embodiment 1. In embodiments 1 to 3, the laminating position of the electric insulation part is the same as a laminating position of an electric insulation part in an adjacent layer unit. However, it is preferable that the laminating positions of the electric insulation parts in the adjacent layers do not overlap as shown in Fig. 5. More preferably, the lamination is performed while periodically changing lamination positions. The laminating positions of the electric insulation parts in the adjacent layers are set different from each other, thereby reducing unevenness generated by the electric insulation parts. Thus, disconnection of the internal electrode and occurrence of short circuit can be prevented. In embodiments 1 and 2, the thickly laminated dielectric layer is etched to flatten the surface of the laminated body. The other method such as laser ablation, namely a method of physically evaporating the surface of the laminated body, can be also used. A combination of the methods can be also used. The degree of the flattening in the present invention is required to be simply enough to prevent the disconnection of internal electrode 11 or short circuit between layers from being caused by deep recessing of electric insulation part 13. The present invention provides a manufacturing method allowing the improvement of the product yield of a small multi-layer capacitor having high capacity.